Wavelet Transform-Based Transient Current Analysis for Detection of Gate-Oxide Shorts in CMOS

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Abstract

In this paper, we present a novel integrated method for testing gate-oxide shorts due to pinhole defects in the gate oxide of CMOS circuits using a wavelet transform-based transient current (i_{DDT}) analysis technique. Wavelet transform has the property of resolving events in both time and frequency domains unlike Fourier transform which decomposes a signal in frequency components only. The proposed method is based on switching the CMOS gate, monitoring the wavelet transform of the transient current and comparing it to the one of the defect-free gate. The MOS transistor is modeled using a two-dimensional non-linear split model. Simulation results on the circuit under test show that wavelet transform has higher fault detection sensitivity than Fourier or peak-current value comparison methods and hence, can be considered very promising for defect oriented testing of gate-oxide shorts.

Keywords: gate-oxide shorts, i_{DDT}, wavelet transformation, leakage, process variation.

1. Introduction

Gate-Oxide Shorts (GOS) in nanometer technologies have an increasing impact on the integrated circuit production yield due to the reduction of the feature sizes, including the thickness of the oxide. The detection of GOS has become a challenging issue since GOS cannot be easily detected using traditional testing techniques. GOS exhibit a complex behavior [1] which cannot be easily modeled. In the past few years, GOS were addressed by many researchers [1-20]. To improve GOS defect coverage, test methods based on the quiescent power supply current (I_{DDQ}) have been proposed such as the one in [1], while others proposed delay testing such as [17, 19]. However, with nanometer technologies the total background leakage current is rising sharply and as a result it is degrading the quality of I_{DDQ} tests. New test methodologies are therefore needed. Techniques based on monitoring transient supply currents (i_{DDT}) provide a good alternative as shown in [21-25]. I_{DDT}-based test methods offer many advantages such as detecting defects that can escape traditional methods. GOS have a noticeable effect on i_{DDT}. A novel technique was proposed in [28] that uses a peak current comparison of transient response. This technique shows good defect coverage but fails for large defect resistance values.

The threshold-based i_{DDT} testing technique is very useful when the transient current levels are known in advance and do not change from one chip to another similar chip. However, this is not the case when process parameters vary and leakage levels change. As an example, circuit simulation of a CMOS inverter using 20 different process parameters, all corresponding to the same IBM 0.13 micron process, show that the peak value of i_{DDT} varies, depending on the process, between 129 μA and 162 μA. This variation makes it virtually impossible to set a single threshold, since a peak current level of, say 140 μA, may be perfectly acceptable in one process, but may indicate a serious fault in another.

In this paper we apply the wavelet transform to i_{DDT} to detect random GOS defects at different locations over the gate plate and with different resistor values that model the severity of the short. We assess the detection capability of i_{DDT} by performing fault simulations on a CMOS inverter. Also, we show that by using a normalization procedure we can use a single threshold for all processes. The rest of the paper is organized as follows: in Section 2 we present the GOS model considered. In Section 3 we give an overview of wavelet transforms, and in Section 4 we introduce the wavelet transform transient current testing method, and show the simulation results. In Section 5 we discuss the effects of process variation and we conclude in Section 6.

2. GOS Modeling

In order to assess the GOS detection capability of i_{DDT}, we consider the two-dimensional non-linear split model proposed in [6]. A non-defective MOS transistor is represented by a two-dimensional array of MOS transistors with *m* lines and *n* columns. There are *n* + 1 transistors in every line and *m* – 1 transistors in every column, giving rise to a total number of $m(n+1) + n(m-1)$ transistors and $m \times n$ nodes as illustrated in Figure 1 [1] where $m = n = 5$. It should be noted that higher accuracy is obtained with a larger number of lines and columns. In our case, we have chosen an array of 5×5 with 50 transistors in total. If all MOSFETs are minimum length transistors, the resulting transistor is larger than a minimum length transistor, which represents the major limitation for the use of this model since it cannot be used to model minimum length transistors.

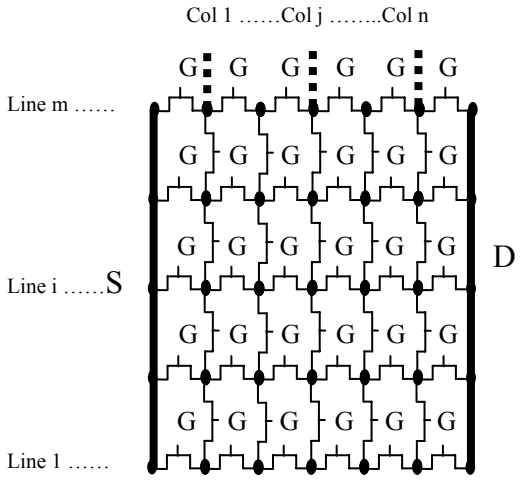

Figure 1: Non-linear split model [1]

In this model a GOS defect is represented by a resistor placed between the common gate and a node in the network as illustrated in Figure 2 [17].

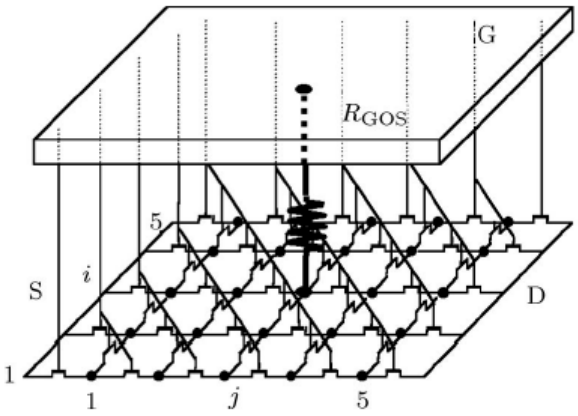

Figure 2: GOS modeling in the split model [17]

3. An Overview of Wavelet Transform

The wavelet transform is a mathematical operation that decomposes a signal simultaneously into time and frequency components [29, 30]. Wavelets have advantages over traditional Fourier methods in analyzing physical situations where the signal contains discontinuities and sharp spikes [31]. The Continuous Wavelet Transform (CWT) of a signal *x(t)* with respect to a wavelet is defined as:

$$X_{w(a,b)} = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} x(t) \psi^* \left(\frac{t-b}{a} \right) dt$$

Where *a* is a positive real number that represents the scale, and *b* is the translational value. Moreover, $\psi(t)$ is a continuous function in both the time domain and the frequency domain called the mother wavelet and * represents the operation of complex conjugate.

4. Testing Method and Results

The criterion that we use to decide whether a circuit under test (CUT) is defective is based on monitoring the wavelet transform of the transient power supply current, i_{DDT}. The wavelet transform of the transient current curve in the CUT is compared to that of the fault-free circuit. The comparison is accomplished through the use of normalized RMS defined in [30] as:

$$\sqrt{\frac{1}{N} \sum_{i=1}^{N} \left(\frac{F_i - G_i}{G_i} \right)^2}$$

Where F_i represents the wavelet coefficients of the faulty circuit, while G_i represents those of the good circuit.
If the normalized RMS of the CUT current wavelet transform coefficients exceeds the one of a good circuit by more than an empirically-determined threshold (10% in this case), the circuit is considered defective. The same technique was then performed using DFT (Discrete Fourier Transform) on the CUT and the good circuit, so that to prove the superiority of the wavelet transform method. The results were also compared with another technique suggested in [28] based on comparing the peak value of the transient current of the defected circuit to that of the defect-free circuit.

4.1 Experimental Setup

All simulations were performed using HSpice and the process parameters used are based on an IBM 0.13 micron process obtained from the MOSIS website [26]. We consider an inverter with the NMOS transistor having the GOS. The NMOS is a 5×5 array with 50 transistors in total, all of minimum length. The first step is to match this network of transistors with a single NMOS transistor. This was done by matching the drain current characteristics. Then we inject GOS faults at all possible locations, i.e. between the common gate and all

internal nodes of the model. The resistor values used are between 1 Ω and 30 KΩ. To simulate a realistic environment, the input to the inverter under test is buffered through two static inverters and the output is connected to four static inverters as a load, as shown in Figure 3. The buffers and fanout inverters are supplied from a different power supply than the CUT in order to isolate the effect of the defective inverter on i_{DDT}. The input of the circuit is switched and i_{DDT} is monitored. After the binary trace files are generated by HSpice, the next step is to process them, by first extracting the useful drain current data, and then applying a wavelet transform as well as a Fourier transform on the same dataset. Then, the normalized RMS values are calculated as described above. MATLAB HSpice toolbox [32] was utilized to parse HSPICE binary files into MATLAB. Then several MATLAB scripts were developed to parse the files and process the datasets using wavelet and Fourier transforms. The mother wavelet function used is "Meyer" (see Figure 4) reported in literature to be the most sensitive for fault detection, while the worst is the "Mexican Hat" function.

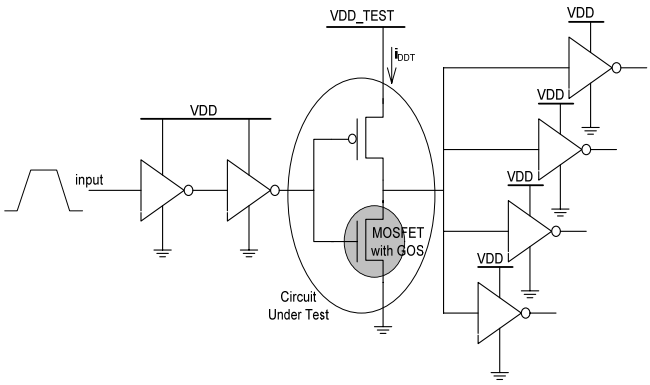

Figure 3: Test Setup

4.2 Results

We study the influence of the resistor value and the influence of the resistor location on the wavelet transform i_{DDT} detection of the GOS fault. For the resistor location, we insert a resistor of 1 KΩ between the common gate and all internal nodes. The nodes are referred to as (i, j) where i and j vary between 1 and 5. The results are shown in Table 1 where the first column indicates the node location while the second column indicates the normalized RMS of the difference of the wavelet transform of the transient current i_{DDT} between the defective circuit and the fault-free one. It can be seen that the RMS values are all above 23% and hence all such defects can be detected using the wavelet transform technique. The third column shows the normalized RMS of the difference between the Fourier transforms of the transient current, while the fourth column shows the percentage difference between current peak values as reported in [28]. It can be observed that the wavelet-based method has significantly better sensitivity than the DFT method. The average sensitivity for wavelet transform is about 50 times than that of DFT.

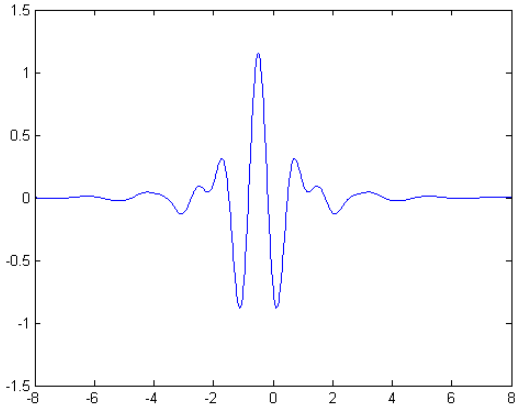

Figure 4: The Meyer mother wavelet function

Concerning the influence of the resistor value, we insert a resistor between the common gate and the central node of the model and vary the resistor value from 30 KΩ down to 1 KΩ in steps of 2 KΩ. Also the values of 750, 500, 250 and 1 Ohm were tested. The results are shown in Table 2. We can notice that using the wavelet technique, all defects including those modeled with high resistance values were successfully detected, but this was not the case when using the peak current technique [28]. We can see that for two resistor values that are relatively large (28 KΩ and 30 KΩ) the percentage differences in the fourth column are below 10% which means that these shorts cannot be detected using the peak-current value comparison technique while they are detected using the wavelet analysis. Note that when we used the "Mexican Hat" mother wavelet instead of "Meyer" the results deteriorated which is consistent with the results presented in [30].

5. Effect of Process Variation

The absolute setting of the threshold margins that were used in the simulations are actually process-dependent and may not work for another process run. This in fact is a limitation of threshold-based current testing in general.

To overcome this limitation, and mask the changes in the process parameters, we propose to normalize the total current response of the circuit under test using the normalization procedure presented in [27], which worked well for static CMOS circuits and which is briefly reviewed below.

Table 1: Influence of resistor location

Node	NRMS-wavelet	NRMS-DFT	% Diff. peak current
(1,1)	31	0.49	30.77
(1,2)	23	0.52	27.88
(1,3)	23	0.6	25.96
(1,4)	23	0.61	24.04
(1,5)	23	0.59	24.04
(2,1)	48	0.52	36.54
(2,2)	27	0.54	34.62
(2,3)	25	0.59	30.77
(2,4)	25	0.6	28.85
(2,5)	24	0.6	27.88
(3,1)	53	0.54	37.50
(3,2)	28	0.52	36.54
(3,3)	26	0.56	32.69
(3,4)	58	0.58	29.81
(3,5)	25	0.61	27.88
(4,1)	49	0.52	37.50
(4,2)	27	0.54	35.58
(4,3)	25	0.59	31.73
(4,4)	25	0.6	28.85
(4,5)	24	0.6	27.88
(5,1)	28	0.49	33.65
(5,2)	23	0.52	29.81
(5,3)	23	0.6	26.92
(5,4)	29	0.61	25.96
(5,5)	23	0.59	25.00

We normalize the total current response of the CUT using the current values from a simple good circuit (which we will refer to as *SGT*) embedded in the chip under test, and the current values of the same SGT embedded in a golden chip, known to be defect free. The SGT can be as simple as a single inverter, which is embedded in all chips that will be tested. We make no assumptions about the process of the golden chip; all we require is the knowledge that the golden chip is defect-free. To normalize the response of a CUT, we use the following equations:

$$S_N = \left[\frac{S_{CUT}}{S_{SGT}}\right]_{\text{in process of CUT}} \times S_{REF}$$

where S_N is the normalized spike, S_{CUT} is the spike value in CUT, S_{SGT} is the spike value of the SGT circuit in the CUT, and S_{REF} is the spike value of the SGT circuit embedded in the golden chip.

Table 2: Influence of resistor value

R (Ω)	NRMS-wavelet	NRMS-DFT	% Diff. peak current
30k	13	0.37	8.65
28k	14	0.38	9.62
26k	14	0.41	10.58
24k	15	0.44	11.54
22k	16	0.41	12.50
20k	17	0.43	12.50
18k	18	0.5	13.46
16k	19	0.5	15.38
14k	20	0.58	16.35
12k	20	0.63	19.23
10k	24	0.7	21.15
8k	23	0.63	25.00
6k	24	0.54	28.85
4k	25	0.53	30.77
2k	26	0.55	31.73
1k	26	0.56	32.69
750	26	0.56	32.69
500	28	0.56	32.69
250	25	0.56	32.69
1	25	0.56	33.65

In order to model leakage, we add another inverter powered from the VDD supply, and we set its input to a value slightly lower than the threshold voltage. This small input voltage will cause a steady-state sub-threshold current to flow between the VDD supply and GND. In a similar manner to the above, we normalize the leakage value using:

$$L_N = \left[\frac{L_{CUT}}{L_{SGT}}\right]_{\text{in process of CUT}} \times L_{REF}$$

where L_N is the normalized leakage, L_{CUT} is the leakage value in CUT, L_{SGT} is the leakage value of the SGT circuit in the CUT, and L_{REF} is the leakage value of the SGT embedded in the golden chip.

We note here that the values of S_{REF}, L_{REF}, S_{SGT}, and L_{SGT} are independent of the input vectors that are applied for testing purposes. They are determined once, at the start of the chip testing procedure.

For a certain test vector pair, the threshold for i_{DDT} testing is set at $I_{TH} = L_{GLD} + 1.1 \times S_{GLD}$, where L_{GLD} is the leakage value, and S_{GLD} is the spike value, both in the golden chip. This value of I_{TH} is vector-dependent, and is now compared to $S_N + L_N$, calculated from the vector-dependent S_{CUT} and L_{CUT}. Values of $S_N + L_N$ higher than I_{TH} indicate the presence of a fault.

By applying this procedure, *all* defects that were previously detected using different process-dependent margins, are now detected using a single "standard" threshold value. Table 3 shows the normalized NRMS for the wavelet transform when the process is varied.

Table 3: Influence of process variation

Process	NRMS-wavelet
T49S	27
T4BJ	32
T51D	25
T51P	26
T51PL	29
T51R	28
T55R	26
T57J	26
T58A	28
T59M	30
5BC	31
T5BCD	32
T65U	23
T68A	26
T68AL	22
T68V	23
T6AS	31
T6ASD	29
T72W	25
T72WD	27

It is worth mentioning at this point that similar to other i_{DDT}-based techniques, the performance of the proposed method deteriorates as the size of the CUT increases. This problem has been addressed previously, and one possible solution is the partitioning of the circuit into clusters of manageable size.

6. Conclusion

In this paper we proposed a new testing method for gate-oxide shorts based on the wavelet transform of the transient power supply current, i_{DDT}. We assessed the effectiveness of this method with a realistic inverter circuit using an array model for the defective MOSFET. The results show a very high rate of detection for GOS faults that cannot be otherwise detected using traditional testing techniques and Fourier transforms, regardless of the short value or the short location. We also showed that by using a simple normalization procedure, the method becomes immune to leakage and process variation, and a single threshold margin can be used for all processes.

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